CLAIMS

1. A phase locked loop (PLL) circuit comprising:

a phase detector comparing an input signal to a feed back signal, the phase detector providing an error signal,

a low pass filter defining a filter output,

a voltage controlled oscillator accepting the output from the low pass filter and output the feedback signal,

at least two charge pumps that each output a driving signal to the low pass filter, wherein the driving signal is responsive to the error signal,

a lock detector that accepts the error output and in response outputs at least one lock signal, wherein the one lock signal represents an indication of a coarse lock,

a reference generator that accepts the first lock signal and in response outputs one reference signal to one charge pump, wherein the reference signal controls the charge pump, and

wherein when the at least two charge pumps provide a signal to the low pass filter the PLL loop bandwidth is higher than when one of the at least two charge pump is inactive.

2. The phase locked loop circuit of claim 1 wherein the at least two charge pumps are each arranged to accept a reference current and output a current to the low pass filter.

3. The phase locked loop circuit of claim 2 wherein the at least two charge pumps are each arranged to accept the same reference current but output different currents to the low pass filter.

4. The phase locked loop circuit of claim 2 wherein the at least two charge pumps are each arranged to accept different reference currents and output different currents to the low pass filter.

5. The phase locked loop circuit of claim 4 wherein the reference source comprises a a first reference current source driving one charge pump, and a second reference current source driving a second charge pump, and wherein the second reference current source is larger than the first reference current source.

6. The phase locked loop of claim 5 wherein the second current source is selected on or off by the coarse lock signal from the lock detector.

7. The phase locked loop of claim 1 wherein the first lock signal is latched.

8. The phase locked loop of claim 1 wherein the reference generator comprises:

first, second and third reference current sources, where the first reference current source has lower magnitude than the second reference current source which has a lower magnitude than the third reference current source, and wherein the lock detector comprises at least two lock signals, a coarse lock signal that controls the third reference current source, and a second lock signal that controls the second reference current source.

9. The phase locked loop of claim 1 wherein the lock detector comprises:

at least one comparator,

a circuit that averages the error signal, the averaged error signal connects to an input of the at least one comparator,

a voltage divider circuit arranged to provide a different trigger voltage to the second input of the at least one comparator, wherein when the average error signal reaches the trigger voltage of each comparator, the lock signal disables the corresponding reference current source, thereby reducing the loop gain of the phase locked loop.

10. A phase locked loop that includes a phase detector providing an error signal to a charge pump, wherein the charge pump in response outputs a current into a low pass filter that outputs a signal to a voltage controlled oscillator, whose output is divided thereby producing a feed back signal that is compared to an input signal in the phase detector, further comprising a lock detector that provides a coarse lock signal indicating that a

coarse lock state has been reached for the PLL, and at least one additional charge pump that defines an output current into the low pass filter, the additional charge pump accepts and is controlled on or off by the coarse lock signal, wherein when the additional charge pump is off the loop bandwidth of the phase locked loop is lowered.

11. The phase locked loop of claim 10 further comprising additional charge pumps and lock detectors that output additional corresponding lock signals to the additional charge pumps, the additional lock signals indicating finer and finer lock conditions of the phase locked loop, wherein as the phase locked loop approaches closer to the finest lock condition, the additional lock signals incrementally turn off the corresponding charge pumps to incrementally reduce the phase locked loop bandwidth.

12. The phase locked loop of claim 10 further comprising a reference current arranged to accept the coarse lock signal and provide a reference current to the charge pump that controls the charge pump output current, wherein when the coarse lock signal is not asserted the reference current drives the charge pump to output a current to the low pass filter, and when the coarse lock signal is asserted turning off the reference current that in turn turns off the charge pump current to the low pass filter.

13 A method of operating a phase locked loop, wherein the loop contains a low pass filter with an output driving a voltage controlled oscillator that outputs a signal that is divided forming a feedback and fed back to a phase detector that compares the feedback signal to an input signal, the phase detector outputting an error signal, wherein the error signal ultimately drives a current via multiple charge pumps into the low pass filter, the method comprising the steps of:

comparing the error signal to reference levels, wherein the reference levels indicate degrees of coarser and finer lock states of the phase locked loop, wherein, in response to the error signal reaches the corresponding reference level,

adjusting the current from the charge pumps so that the loop gain of the phase locked loop is reduced as finer locks are reached.,